TRANSMITTAL OF APPEAL BRIEF

Docket No.
M4065.0244/P244

In re Application of: James S. Cullum et al.

Application No.	Filing Date	Examiner	Group Art Unit
09/575,456	May 22, 2000	James K. Trujillo	2116

Invention: METHOD AND APPARATUS FOR ADJUSTING DATA HOLD TIMING OF AN OUTPUT CIRCUIT

TO THE COMMISSIONER OF PATENTS:

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Dated: April 4, 2005

Thomas J. D'Amico
Attorney Reg. No. : 28,371
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 828-2232

Docket No.: M4065.0244/P244
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:
James S. Cullum et al.

Application No.: 09/575,456 Art Unit: 2116

Filed: May 22, 2000 Examiner: James K. Trujillo

For: METHOD AND APPARATUS FOR ADJUSTING DATA HOLD TIMING OF AN OUTPUT CIRCUIT

APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief - Patents
Randolph Building
Alexandria, VA 22314

Dear Sir:

This is an Appeal Brief pursuant to 35 U.S.C. § 134 and 37 C.F.R. §§ 41.31 et seq. from the final rejection of claims 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52 of the above-identified application. The Notice of Appeal was filed on February 2, 2005. The fee for submitting this Brief in accordance with 37 C.F.R. § 1.17(c) is attached. Any deficiency in the fees associated with this Brief should be charged to Deposit Account No. 04-1073.

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is MICRON TECHNOLOGY, INC., a corporation organized under and pursuant to the laws of the State of Delaware, and the assignee of this application.

II. RELATED APPEALS AND INTERFERENCES

There are no other known appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Current Status of Claims

1. Claims canceled: 3, 4, 7-9, 14, 17, 18, 21-23, 28, 31, 32, 35-37, 44 and 48

2. Claims withdrawn from consideration but not canceled: none

3. Claims pending: 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52

4. Claims allowed: none

5. Claims rejected: 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52

B. Claims on Appeal

The claims on appeal are claims 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52.

IV. STATUS OF AMENDMENTS

A final Office Action was mailed February 5, 2004. In response to the final Office Action, Appellants filed a Request for Continued Examination and an Amendment on May 5, 2004. A non-final Office Action was mailed June 10, 2004. In response, Appellants filed a Request for Reconsideration on September 9, 2004. A final Office Action was mailed November 4, 2004. Appellants filed a Notice of Appeal on February 2, 2005. No amendments have been submitted subsequent to the November 4, 2004 final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a data output apparatus, a processor based system, and a memory device, each having a plurality of output circuits 13a, 13b . . . 13n each of which receives and outputs a respective data signal DQ0, DQ1 . . . DQn, each output circuit operating in response to a respective applied clock signal; a clock source 17 for supplying a first clock signal; and a plurality of adjustable delay circuits 21a, 21b . . . 21n for receiving the first clock signal, each of the adjustable delay circuits providing a respective delayed first clock signal to a respective one of the plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one fuse element for programming such that each of the respective data signals is output by the plurality of output circuits at substantially the same time. (Application at page 4, line 15 – page 5, line 6; page 6, line 17 – page 7, line 2; with numeric reference to FIG. 3, reproduced below).

As operating speeds of memory devices, and other data output devices have increased, it has become increasingly important to synchronize the outputs of all bits of data at the output circuits. The invention achieves this by tailoring the clock signal

received by each output circuit in order to avoid data output skew across all bits of the output data word.

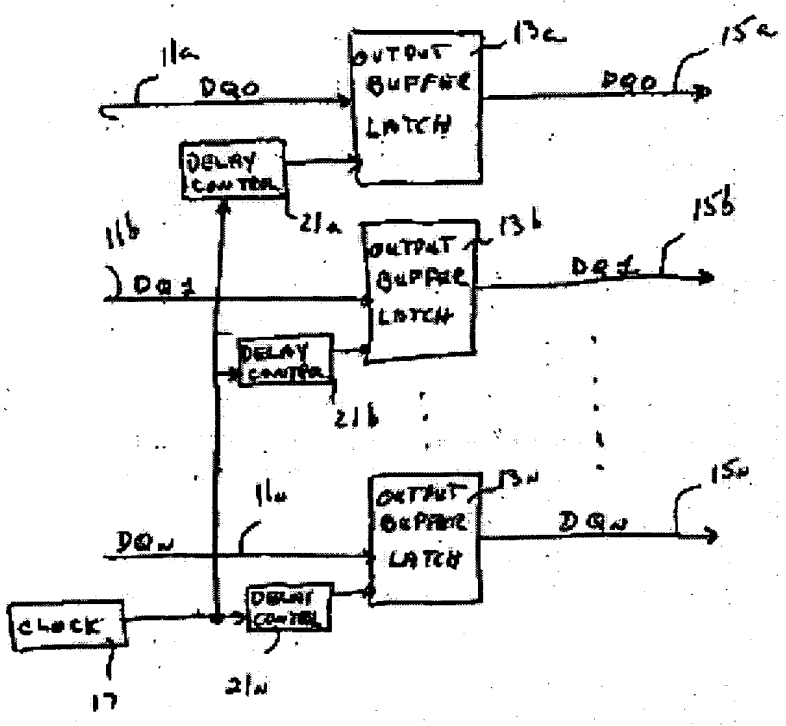

FIG. 3

The invention also relates to a data output apparatus, a processor based system, and a memory device, each having the same features described above except that each programming circuit contains at least one anti-fuse element instead of a fuse element. (Application at page 6, lines 1-4).

The invention further relates to a method of providing data output signals, the method comprising receiving a plurality of data output signals DQ0, DQ1 . . . DQn at respective output circuits 13a, 13b . . . 13n; operating the output circuits in response to respective applied clock signals to make the data output signals available at respective outputs of the output circuits; providing a first clock signal; generating each

of the respective applied clock signals from the first clock signal, each of the respective applied clock signals having a respective adjustable delay relative to the first clock signal; programming each respective adjustable delay by modifying a conductive state of at least one of a fuse element and an anti-fuse element to select a delay rate; and adjusting the delay of each of the respective applied clock signals such that the data output signals DQ0, DQ1 . . . DQn are output from the respective outputs of the output circuits 13a, 13b . . . 13n at substantially the same time. (Application at page 4, line 15 – page 5, line 6; page 6, line 17 – page 7, line 2; with numeric reference to FIG. 3, reproduced above).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of Ashuri (U.S. Patent No. 5,652,530) ("Ashuri").

VII. ARGUMENT

A. CLAIMS 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52 ARE PATENTABLE OVER APPLICANT'S ADMITTED PRIOR ART IN VIEW OF ASHURI (U.S. PATENT NO. 5,652,530)

The Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52 since a person of ordinary skill in the art at the time of the invention would not have found any suggestion to combine the references together, nor would such a person be motivated to do so. Further, even if there were some motivation to combine these two reference, which there is none, neither AAPA nor Ashuri, whether considered alone or in combination, teach or suggest all the limitations of claims 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52.

For example, claims 1, 15, 29 and 49-51 each recite, *inter alia*, a "plurality of output circuits" each of which outputs a respective data signal, a clock source and "a plurality of adjustable delay circuits" for receiving a first clock signal and "for providing a respective delayed first clock signal to a respective one of said plurality of output circuits." Claims 1, 15, 29 and 49-51 also recite, *inter alia*, that "each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal [. . .] such that each of said respective data signals is output by said plurality of output circuits at substantially the same time."

Claim 41 recites receiving a plurality of data output signals, providing a first clock signal, generating respective applied clock signals and "adjusting the delay of each of said respective applied clock signals such that the data output signals are output from . . . respective outputs of said output circuits at substantially the same time." Neither AAPA nor Ashuri, taken alone or in combination, teach or suggest the combinations defined in claims 1, 15, 29, 41 and 49-51, which include the above-quoted limitations.

AAPA discloses a conventional data output circuit in which a clock signal originating from clock source 17 is provided to output circuits 13a, 13b . . . 13n through a single delay circuit 19. Due to unequal circuit path lengths of clock signal lines and other timing aberrations caused by circuit topology within a chip, at higher clocking speeds, it was becoming increasingly difficult to insure that the output data signals DQ0, DQ1 . . . DQn were being applied to respective data output lines at substantially the same time, that is, without timing skew of the individual bits of a data word. (Application at page 2, line 11 – page 3, line 8; with numeric reference to FIG. 1, reproduced below). The AAPA is incapable of addressing timing skew across all output bits of a data word due to the different clock signals and their associated timing skews, applied to each of the output data latches 13a, 13b . . . 13n.

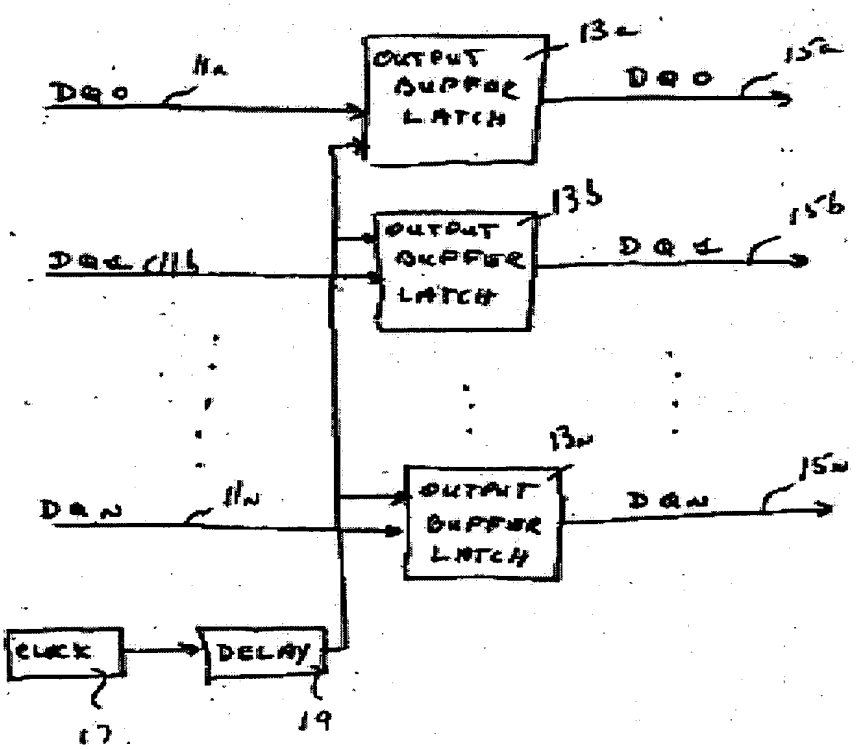

FIG. 1

The final Office Action acknowledges that AAPA does not disclose a plurality of adjustable delay circuits for receiving the first clock signal, each of the adjustable delay circuits providing a respective delayed first clock signal to a respective one of the plurality of output circuits. (Final Office Action dated November 4, 2004 at page 2). The final Office Action also acknowledges that AAPA does not disclose that each of a plurality of adjustable delay circuits contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one fuse element for programming. (Final Office Action dated November 4, 2004 at pages 2-3). In summary, the final Office Action acknowledges that AAPA merely discloses using a single delay for a clock for a plurality of output circuits wherein each output circuit has different data signals

coupled to their respective inputs. (Final Office Action dated November 4, 2004 at page 3).

The final Office Action then points to Ashuri and although it acknowledges that Ashuri discloses only a single output circuit having an adjustable delay 315 providing a delayed first clock signal 321 to an output circuit 350, for some reason, the final Office Action apparently takes the position that the combination of AAPA and Ashuri discloses the inventions defined by claims 1, 15, 29, 41 and 49-51. Final Office Action dated November 4, 2004 at page 3; with numeric reference to FIG. 3 of Ashuri, reproduced below).

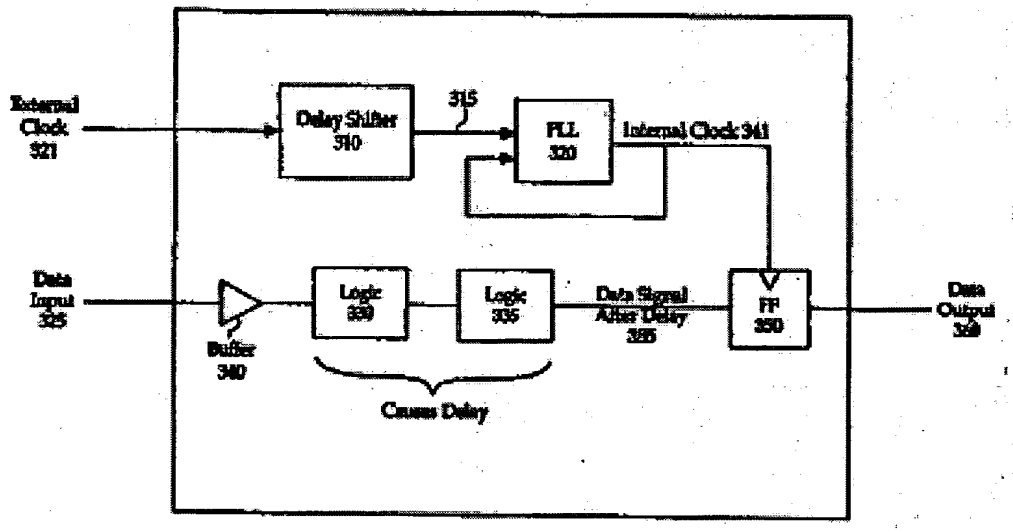

FIG. 3 of Ashuri

Ashuri, however, does not even contemplate the same problem that is addressed by the present invention – *i.e.*, preventing timing skew of the individual bits of an output data word. Rather, Ashuri is directed to delaying a clock signal 321 so as to match a delay realized by a data signal 325 passing through many logic gates on its

way to being sampled at a flip-flop 350. That is, Ashuri attempts to prevent premature sampling of data at a flip-flop 350 by delaying the clock signal that triggers the sampling until such time as the data signal is actually present for sampling at the flip-flop. (Ashuri at column 1, lines 43-60, with numeric reference to FIG. 3 of Ashuri, reproduced above). Ashuri is *not* directed to preventing timing skew of multiple bits at an output word. The only similarity between Ashuri and the AAPA is that they both introduce a delay into a clock signal – however, as described above, they do so for very different reasons and, further, the AAPA does *not* do so in a manner adequate enough to avoid timing skew at the output word. Thus, a person of ordinary skill in the art at the time of the invention would have no motivation to combine AAPA and Ashuri and arrive at the inventions defined by claims 1, 15, 29, 41 and 49-51. Not only is there not any indication within either reference that they could be combined to arrive at the claimed inventions, but a person of ordinary skill in the art would have no reason to even consult Ashuri since it is directed to correcting an entirely different problem. Rather, the final rejection is using impermissible hindsight by using the claims of the present invention as a road map to improperly combine the references. *See Ex parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. App. 1985); M.P.E.P. § 2144. At least for these reasons, claims 1, 15, 29, 41 and 49-51 are allowable over AAPA and Ashuri.

Further, as acknowledged by the final Office Action, Ashuri does *not* teach or suggest *a plurality of adjustable delay circuits wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to a first clock signal* such that a plurality of data signals are output *by a respective plurality of output circuits at substantially the same time.* Therefore, even if there were some motivation to combine the AAPA and Ashuri, which there is none, the two references when combined still do not disclose all of the limitations of claims 1, 15, 29, 41 and 49-51. This is another reasons why the rejection should be reversed.

Claims 2, 5, 6, 10-13, 16, 19, 20, 24-27, 30, 33, 34, 38-40, 42, 43 and 45-47 depend from claims 1, 15, 29 and 41 and are allowable at least for the reasons mentioned above in connection with claims 1, 15, 29 and 41 and also on their own merit since neither AAPA nor Ashuri, taken alone or in combination, teaches or suggests their respective inventive combinations.

For example, claim 2, which depends from claim 1, further recites that "each of the output circuits has an associated output data hold time, the timing of which is adjustable by the delay of a respective delay circuit." As mentioned above, neither AAPA nor Ashuri, either taken alone or in combination, teaches or suggests a plurality of respective delay circuits, much less that the delay of the plurality of delay circuits adjust the timing of an associated data hold time of the plurality of output circuits. At least for these reasons, the rejection of claim 2 should also be reversed.

In another example, claim 5 depends from claim 2 and further recites "a plurality of data output terminals respectively connected to said output circuits," and that "the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident." As mentioned above, neither AAPA nor Ashuri, either taken alone or in combination, teaches or suggests a plurality of respective adjustable delay circuits, much less that the delay of each of the adjustable delay circuits is adjusted such that the data hold time as seen at the respective output terminal is substantially coincident. At least for these reasons, the rejection of claim 5 should also be reversed.

VIII. CONCLUSION

For the reasons given above it is respectfully submitted that the final rejection of claims 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52 is

improper. Accordingly, Appellant requests reversal of all rejections by this honorable Board.

Dated: April 4, 2005

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No. 28,371
Salvatore P. Tamburo
Registration No. 45,153
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700

Attorneys for Appellants

APPENDIX A

1. A data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

2. A data output apparatus as in claim 1 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

5. A data output apparatus as in claim 2 further comprising a plurality of data output terminals respectively connected to said output circuits, and

wherein the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident.

6. A data output apparatus as in claim 1 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

10. A data output apparatus as in claim 6 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

11. A data output apparatus as in claim 10 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

12. A data output apparatus as in claim 1 wherein said output circuits are output buffer circuits.

13. A data output apparatus as in claim 1 wherein each of said output circuits receives and outputs a respective data signal from a memory array.

15. A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

16. A processor based system as in claim 15 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

19. A processor based system as in claim 16 wherein each of said output circuits is coupled to a respective output terminal and the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident.

20. A processor based system as in claim 15 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing a different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

24. A processor based system as in claim 20 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

25. A processor based system as in claim 24 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

26. A processor based system as in claim 15 wherein said output circuits are output buffer circuits.

27. A processor based system as in claim 15 wherein each of said output circuits receives and outputs a respective data signal from a memory array.

29. A memory device comprising:

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, each programming circuit containing at least one fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

30. A memory device as in claim 29 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

33. A memory device as in claim 30, further comprising a plurality of data output terminals respectively connected to said output circuits.

34. A memory device as in claim 29 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

38. A memory device as in claim 34 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

39. A memory device as in claim 38 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

40. A memory device as in claim 29 wherein said output circuits are output buffer circuits.

41. A method of providing data output signals comprising:

receiving a plurality of data output signals at respective output circuits;

operating said output circuits in response to respective applied clock signals to make said data output signals available at respective outputs of said output circuits;

providing a first clock signal;

generating each of said respective applied clock signals from said first clock signal, each of said respective applied clock signals having a respective adjustable delay relative to said first clock signal;

programming each respective adjustable delay by modifying a conductive state of at least one of a fuse element and an anti-fuse element to select a delay rate; and

adjusting the delay of each of said respective applied clock signals such that the data output signals are output from said respective outputs of said output circuits at substantially the same time.

42. A method as in claim 41 wherein said data output signals are available at the outputs of said output circuits for a respective data hold time, the timing of said data hold time for each of said output circuits being independently adjusted by adjusting the delay of a respective applied clock signal.

43. A method as in claim 42 wherein the amount of delay of each of said applied clock signals is programmable.

45. A method as in claim 42, wherein each of said output circuits is connected to a respective output terminal, said method further comprising adjusting the delay of said applied clock signals such that the data hold time, as seen at each of said output terminals, is substantially coincident.

46. A method as in claim 45 wherein said terminals are exterior terminals of an integrated circuit package containing said output circuits.

47. A method as in claim 41 wherein each of said applied clock signals is generated by receiving said first clock signal and subjecting said received first clock signal to a selected one of a plurality of signal delays.

49. A data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each of said output circuits operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming such that said data signals are output by said plurality of output circuits at substantially the same time.

50. A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each of said output circuits operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

51. A memory device comprising:

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

52. A data output apparatus as in claim 1, wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing different respective delay to a signal applied thereto; and,

a switch circuit for configuring said delay elements to provide a selected delay to the delayed first clock signal.